Logic Mind Technologies Pvt Ltd. Bangalore,
8123668066 / 9036159759 / 9108159759

No	CODE	TITLE	DOMAIN	YEAR
1	LMVLSI-01	A Modified Partial Product Generator for Redundant Binary Multipliers	Area Efficient	2016
2	LMVLSI-02	Multiplier less Unity-Gain SDF FFTs	Area Efficient	2016
3	LMVLSI-03	LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter	Area Efficient	2016
4	LMVLSI-04	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	Area Efficient	2016
5	LMVLSI-05	Hybrid LUT/Multiplexer FPGA Logic Architectures	Area Efficient	2016
6	LMVLSI-06	Low-Complexity First-Two-Minimum-Values Generator for Bit-Serial LDPC Decoding	Area Efficient	2016
7	LMVLSI-07	Design and simulation of Turbo encoder in quantum-dot cellular automata	Area Efficient	2016
8	LMVLSI-08	A New Paradigm of Common Sub expression Elimination by Unification of Addition and Subtraction	Area Efficient	2016
9	LMVLSI-09	A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders	Area Efficient	2015
10	LMVLSI-10	Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations Turbo Decoders	Area Efficient	2015
11	LMVLSI-11	Efficient Circuit for Parallel Bit-Reversal	High Speed	2016
12	LMVLSI-12	A New Fast and Area-Efficient Adder-Based Sign Detector for RNS $\{2^n - 1, 2^n, 2^n + 1\}$	High Speed	2016
13	LMVLSI-13	High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations	High Speed	2016
14	LMVLSI-14	A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler	High Speed	2015
15	LMVLSI-15	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis	High Speed	2015
16	LMVLSI-16	Low-Power Split-Radix FFT Processors Using Radix-2 Butterfly Units	Low Power	2016
17	LMVLSI-17	Design-Efficient Approximate Multiplication Circuits Through Partial Product Perforation	Low Power	2016
18	LMVLSI-18	Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance Operation	Low Power	2016
19	LMVLSI-19	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	Low Power	2016
20	LMVLSI-20	Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding	Low Power	2016

21	LMVLSI-21	Low-Cost and High-Reduction Approaches for Power Droop During Launch-On-Shift Scan-Based Logic BIST	Testing	2016
22	LMVLSI-22	Low-Power Programmable PRPG With Test Compression Capabilities	Testing	2016
23	LMVLSI-23	Design for Testability of Sleep Convention Logic	Testing / Tanner/ Micro wind	2016
24	LMVLSI-24	A Low-Cost Low-Power Ring Oscillator-based Truly Random Number Generator for Encryption on Smart Cards	Matlab + VLSI	2016
25	LMVLSI-25	Graph-Based Transistor Network Generation Method for Super gate Design	Tanner/Micro wind	2016
26	LMVLSI-26	Low-Energy Power-ON-Reset Circuit for Dual Supply SRAM	Tanner/Micro wind	2016
27	LMVLSI-27	Single-Supply 3T Gain-Cell for Low-Voltage Low-Power Applications	Tanner/Micro wind	2016
28	LMVLSI-28	A Single-Ended With Dynamic Feedback Control 8T Sub threshold SRAM Cell	Tanner/Micro wind	2016
29	LMVLSI-29	Designing Tunable Sub threshold Logic Circuits Using Adaptive Feedback Equalization	Tanner/Micro wind	2016
30	LMVLSI-30	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design	Tanner/Micro wind	2016
31	LMVLSI-31	High-Speed, Low-Power, and Highly Reliable Frequency Multiplier for DLL-Based Clock Generator	Tanner/Verilog	2016
32	LMVLSI-32	CORDIC II: A New Improved CORDIC Algorithm	Matlab + VLSI	2016
33	LMVLSI-33	A Scalable Approximate DCT Architectures for Efficient HEVC Compliant Video Coding	Matlab + VLSI	2016
34	LMVLSI-34	Unequal Error Protection Codes Derived from Double Error Correction Orthogonal Latin Square Codes	Error Correction	2016
35	LMVLSI-35	Timing Error Tolerance in Small Core Designs for SoC Applications	Error Correction	2016
36	LMVLSI-36	Low-Complexity First-Two-Minimum-Values Generator for Bit-Serial LDPC Decoding	Matlab + VLSI	2016
37	LMVLSI-37	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks	Error Correction	2016
38	LMVLSI-38	A Voltage Regulator-Assisted Lightweight AES Implementation Against DPA Attacks	Matlab + VLSI	2016
39	LMVLSI-39	A Low-Cost Low-Power Ring Oscillator-based Truly Random Number Generator for Encryption on Smart Cards	Matlab + VLSI	2016
40	LMVLSI-40	Efficient Coding Schemes for Fault-Tolerant Parallel Filters	Matlab + VLSI	2015
41	LMVLSI-41	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT	Matlab + VLSI	2015
42	LMVLSI-42	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	Low Power	2015

43	LMVLSI-43	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis	Low Power	2015
44	LMVLSI-44	Low-Power and Area-Efficient Shift Register Using Pulsed Latches	Low Power	2015
45	LMVLSI-45	Novel Approach to Protect Advanced Encryption Standard Algorithm Implementation Against Differential Electromagnetic and Power Analysis	High Speed	2015
46	LMVLSI-46	Efficient Coding Schemes for Fault-Tolerant Parallel Filters	Error Correction	2015
47	LMVLSI-47	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	Area Efficient	2014
48	LMVLSI-48	Area-Delay-Power Efficient Fixed-Point LMS Adaptive Filter With Low Adaptation-Delay	Area Efficient	2014
49	LMVLSI-49	Improved 8-Point Approximate DCT for Image and Video Compression Requiring Only 14 Additions	Area Efficient	2014
50	LMVLSI-50	Input Vector Monitoring Concurrent BIST Architecture Using SRAM Cells	Testing	2014